Fpga Spice A Simulation Based Power Estimation Framework

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Fpga Spice A Simulation Based

Abstract: In this paper, we developed a simulation-based architecture evaluation framework for field-programmable gate arrays (FPGAs), called FPGA-SPICE, which enables automatic layout-level estimation and electrical simulations of FPGA architectures. FPGA-SPICE can automatically generate Verilog and SPICE netlists based on realistic FPGA configurations and a high-level eTtensible Markup Language-based FPGA architectural description language.

FPGA-SPICE: A Simulation-Based Architecture Evaluation ...

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FPGA-SPICE: A Simulation-Based Architecture Evaluation ...

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FPGA-SPICE: A Simulation-Based Architecture Evaluation ...

simulation-based power estimation framework for FPGAs, called FPGA-SPICE, which supports any FPGA architecture that can be described with an architectural description language. Our power estimation engine automatically generates accurate SPICE netlists according to the FPGA configurations and enables precise power analysis of FPGA architectures.

FPGA-SPICE: A Simulation-based Power Estimation Framework ...

FPGA-SPICE: A simulation-based power estimation framework for FPGAs Abstract: Mainstream Field Programmable Gate Array (FPGA) power estimation tools are based on probabilistic activity estimation and analytical power models.

FPGA-SPICE: A simulation-based power estimation framework ...

FPGA-SPICE: A Simulation-based Power Estimation Framework for FPGAs Tang, Xifan ; Gaillardon, Pierre-Emmanuel ; De Micheli, Giovanni Mainstream Field Programmable Gate Array (FPGA) power estimation tools are based on probabilistic activity estimation and analytical power models.

FPGA-SPICE: A Simulation-based Power Estimation Framework ...

(Gappa-based analysis) and timing violations (in-situ FPGA experiments). • Quantification of speedups and resource savings of a hardware-accelerated SPICE simulator across a variety of circuit benchmarks obtained from academic projects and industrial packages. II. BACKGROUND The SPICE [1] circuit simulator (spice3f5) belongs to a

Enhancing Speedups for FPGA Accelerated SPICE through ...

simulation-based power estimation framework for FPGAs, called FPGA-SPICE , which supports any FPGA architecture that can be described with an architectural description language.

(PDF) FPGA-SPICE: A simulation-based power estimation ...
FPGA-SPICE aims at generating SPICE netlists and testbenches for the FPGA architectures supported by VPR. The SPICE netlists and testbenches are generated according to the placement and routing results of VPR. As a result, SPICE simulator can be used to perform precise delay and power analysis.

Motivation — OpenFPGA 1.0 documentation
All this is too much for SPICE notation, or say better, SPICE wasn’t developed to descibe all of this in any easy way. However, the language VHDL-AMS was designed to deal with such use case. VHDL-AMS is an extension of the VHDL that FPGA and IC-Designer are used to work with.

Beyond SPICE - Analog/Mixed Signal Simulation - HardwareBee
Spatial processing of sparse, irregular, double-precision floating-point computation using a single FPGA enables up to an order of magnitude speedup and energy-savings over a conventional microprocessor for the simulation program with integrated circuit emphasis (SPICE) circuit simulator.

Accelerating the SPICE Circuit Simulator Using an FPGA: A ...
FPGA-SPICE is a simulation-based tool dedicated to accurate power estimation of Field Programmable Gate Arrays (FPGAs) 1. FPGA-SPICE is an extension to the Verilog-To-Routing (VTR) tool suite 2 and is tightly integrated into the Versatile Placement and Routing (VPR) tool.

FPGA-SPICE – LSI
Krzysztof joined Aldec in 2001 and was a key member of the team that developed HES-DVM™, Aldec's FPGA-based simulation acceleration and emulation technology. He has worked in the fields of HDL IP-core verification, testbench automation and design verification for DO-254 compliance gaining practical experience and deep understanding of design verification methodologies, emulation and physical prototyping.

Emulation in FPGA - Aldec
SPICE simulators have the advantages of generality and accuracy over analytical models. For this reason, SPICE simulation results are often selected to check the accuracy of analytical models. Therefore, there is a strong need for a simulation-based power analysis approach for FPGAs, which can support general circuit designs.

OpenFPGA/motivation.rst at master · LNIS ... - GitHub
Integrated directly with NI’s VeriStand & LabView, OPAL-RT’s FPGA-based Power Electronics Add-On (eHS) is a powerful FPGA-based simulation tool for Hardware-in-the-Loop (HIL) testing. Used with controllers for power electronics applications, it enables users to simulate an electric circuit on FPGA automatically, and through a convenient user interface, without having to write the mathematical equations.

FPGA simulator FPGA prototyping eFPGASIM - OPAL-RT
Run SPICE simulation¶. Simulation results. The HSPICE simulator creates an LIS file (*.lis) to store the results. In each LIS file, you can find the leakage power and dynamic power of each module, as well the total leakage power and the total dynamic power of all the modules in a SPICE netlist.

Run SPICE simulation — OpenFPGA 1.0 documentation
NI Multisim (formerly MultiSIM) is an electronic schematic capture and simulation program which is part of a suite of circuit design programs, along with NI Ultiboard. Multisim is one of the few circuit design programs to employ the original Berkeley SPICE based software simulation.

Design and Simulate a Digital Circuit in NI Multisim and ...
SPICE (Simulation Program with Integrated Circuit Empha- sis) [1] is a circuit-simulator used to model static and dynamic analog behavior of electronic circuits. SPICE is part of the SPEC92 Floating-Point benchmarks [2] which is a collection of challenge problems for processors.

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